REMARKS

Title

The title of the inventions was objected to for allegedly being not descriptive. The title has been amended to make it descriptive.

Rejections under 35 USC §102(b)

Claims 10-12 [1] were rejected under 35 USC §102(b) as being anticipated by Beilin et al. (U.S. Patent No. 5,916,453).

Applicant respectfully traverses the rejection.

Claim 10 has been amended to "A method for manufacturing a front-and-back electrically conductive substrate, the method comprising the steps of: preparing a wafer made of a single material having a thickness greater than a height of a plurality of posts to be formed; forming, by a process of anisotropic etching, the plurality of posts having an electrically conductive portion; and filling space between the plurality of posts with an insulating material."

Beilin et al discloses methods of planarizing structures on wafers and substrates by polishing. Beilin et al describes in the relevant portion as follows:

> Referring to FIG. 14, photosensitive layer 112 is removed, and a new photosensitive layer 116 is formed over polish-stop layer 122 to form a composite layer comprising planarizing layer 120, polish-

1. The Examiner inadvertently refers to claims 14-16 throughout the Office Action

> stop layer 122, and photosensitive layer 116. A plurality of apertures 117 are then formed through the composite layer. Apertures 117 are most readily formed by first pattern exposing photosensitive layer 116 to actinic radiation (for example UV light), developing layer 116, and then using layer 116 as an etch mask to transfer the pattern of apertures in layer 116 to layer 120 by a suitable etching process. An anisotropic etching process is preferred, such as for example plasma assisted etching processes. Reactive ion etching (RIE) is one preferred etching process. . . . .

(Col. 6, lines 7-18). Also, Beilin et al describes as follows:

> **Once apertures 117 are formed, they may be filled with material to form post 118 as shown in FIG. 15 with the deposition processes** described above with respect to the first generalized embodiment of the present invention. Thereafter, photosensitive layer 116 is removed, as shown in FIG. 16, and the resulting structure is polished, as shown in FIG. 17. . . . .

(Col. 6, lines 53-59). According to Beilin et al, the posts 118 must be made by deposition processes. Nothing indicates that the posts 118 can be made by anisotropic etching. Also, according to Beilin et al, when the posts are formed, the posts are already in the insulating layer. There is no step of filling space between the plurality of posts with an insulating material.

Beilin et al discloses none of the steps of "preparing a wafer made of a single material having a thickness greater than a height of a plurality of posts to be formed;" "forming, by a process of anisotropic etching, the plurality of posts having an electrically conductive portion;" and "filling space between the plurality of posts with an insulating material," recited in claim 10.

For at least these reasons, claim 10 patentably distinguishes over Beilin et al. Claims 11 and 12, depending from claim 10, also patentably distinguish over Beilin et al for at least the same reasons.

Thus, the 35 USC §102(b) rejection should be withdrawn.

Claim [10] was rejected under 35 USC §102(b) as being anticipated by JP 11-163207 (JP'207).

Applicant respectfully traverses the rejection.

JP'207 discloses a method of manufacturing a semiconductor chip mounting substrate. The Examiner alleges as follows:

> The JP'207 discloses the method of the present application comprising: forming by a process of anisotropic etching a plurality of posts 1's having an electrically conductive portion that has at least a first surface and a second surface that communicate with each other (see Figs. 1a-d); and filling space between the plurality of posts with an insulating material (see Fig. 2b). Note that metal etching process by Ultrasonic wave of the JP'027 represents the anisotropic etching as broadly cited in the present application's claims.

Claim 10 has been amended to recite "preparing a wafer made of a single material having a thickness greater than a height of a plurality of posts to be formed."

According to JP'207, the metal foil has three layers and these layers are made of metals of different etching properties. Thus, the metal foil is not made of a single material.

Therefore, JP'207 does not teach or suggest "preparing a wafer made of a single material having a thickness greater than a height of a plurality of posts to be formed", as recited in claim 10.

For at least these reasons, claim 10 patentably distinguishes over JP'207.

Thus, the 35 USC §102(b) rejection should be withdrawn.

Rejections under 35 USC §103(a)

Claims [10-12] were rejected under 35 USC §103(a) as being obvious over Beilin et al. (U.S. Patent No. 5,916,453) in view of Albrecht et al. (U.S. Patent No. 4,968,585).

Applicant respectfully traverses the rejection.

The Examiner alleged that, even if Beilin et al does not disclose the post being formed by anisotropically etched silicon, Albrechit et al discloses it.

However, as discussed above, Beilin et al not only fail to disclose posts being formed by anisotropically etched silicon, but Beilin et al fail to disclose all the steps of "preparing a wafer made of a single material having a thickness greater than a height of a plurality of posts to be formed;" "forming, by a process of anisotropic etching, the plurality of posts having an electrically conductive portion;" and "filling space between the plurality of posts with an insulating material," recited in claim 10.

Albrecht et al discloses a microfabricated cantilever stylus with integrated conical tip. The abstract describes as follows:

> A cantilever stylus with an integrally formed conical tip is provided for atomic force microscopy AFM. The method for forming a stylus includes forming a circular masking pattern [14] on the surface of a silicon substrate and anisotropically etching the silicon to form a post [18] under the masking pattern. [See Figs. 2-3.] The post [18] is then **isotropically etched to produce a conical silicon tip mold**. [See Fig. 4.] In one embodiment of the invention the silicon substrate and the conical silicon tip mold are thermally oxidized to form a cantilever stylus having including a cantilever arm with a conical tip fixed to its free end. In another embodiment of the invention the silicon substrate and the conical silicon tip mold are coated with a thin film of a dielectric material to form a cantilever stylus with a conical tip. In this embodiment the backside of the stylus is coated with a conductive material and a strong electric field is applied to the tip to cause electromigration of the conductive material to the point of the tip.

(Emphasis and references to drawings added). The microfabricated cantilever stylus of Albrecht et al is rather isotropically etched and it has nothing to do with the "forming, by anisotropic etching the plurality of posts," recited in claim 1. Moreover, nothing in Albrecht et al indicates that the microfabricated cantilever stylus can be related to the front-and-back electrically conductive substrate as recited in claim 1.

For at least these reasons claim 10 patentably distinguishes over Beilin et al. Claims 11 and 12, depending from claim 10, also patentably distinguish over Beilin et al for at least the same reasons.

Thus, the 35 USC §102(b) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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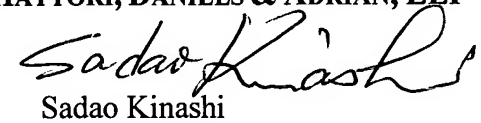

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